Remarks

In the instant Office Action dated September 2, 2008, the following rejection is noted: claims 1-16 stand rejected under 35 U.S.C. § 103(a) over Applicant's Admitted Prior Art (Background and Figures 1 and 2) in view of Baldwin (U.S. Patent No. 5,798,770). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the rejection of claims 1-16 under 35 U.S.C. § 103(a). The rejection relies upon two purported advantages that the skilled artisan would seek as the reason for combining the references. Without these advantages, there is no articulated reason for combining the references. M.P.E.P. § 2141: "The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." The purported advantages are 1) to enhance the performance and flexibility of processing data, and 2) to eliminate unnecessary processing (see instant Office Action response at page 3). The skilled artisan would not attempt to obtain these advantages by implementing the combination asserted by the Office Action because the combination at best does not provide the stated benefits and frustrates attempts to realize such advantages.

The Office Action identifies the combination as a modification of either FIG. 1 or FIG. 2 (Applicant's disclosure) to include the multiplexer of Baldwin. Applicant will address each asserted combination in turn.

Regarding FIG. 2, Applicant's disclosure teaches that the pipeline stages are designed for the desired application by removing unnecessary functional blocks from certain ones of the pipelines (*see, e.g.*, paragraph 006 of the published version of Applicant's disclosure). Accordingly, Applicant does not understand what benefit would be seen by adding aspects of the Baldwin reference as unnecessary functional blocks are taught to be removed from the pipeline stages during design of the processor. Particularly, there does not appear to be any need for the multiplexer of Baldwin and to disable functional blocks of FIG. 2. Moreover, there is no articulated logical explanation as to how performance, flexibility and unnecessary processing are improved when the circuit of FIG. 2 is designed without unnecessary processing elements.

Regarding FIG. 1, Applicant's disclosure teaches that each functional block F1-F6 consumes different amounts of area, cost and power (*see, e.g.*, paragraph 004). These functional blocks are selectively used by appropriately setting parameters for each functional block (*see, e.g.*, paragraph 007). There would be no improvement in flexibility or performance from the addition of aspects from Baldwin because the circuit of FIG. 1 already provides the functionality that forms the basis for the modification in view of Baldwin. More specifically, the processing blocks of FIG. 1 can be selectively implemented using parameter settings, negating any need for the proposed modification. Moreover, adding additional multiplexer circuitry of Baldwin would complicate the processor and, if anything, reduce flexibility/performance of the circuit. The addition of the Baldwin multiplexer and related control circuitry would increase the area, cost and/or power of the processor of FIG. 1. The skilled artisan would not add additional circuitry of Baldwin to perform a function that is already performed by the pipeline of FIG. 1. The pipelines of FIG. 1 already have the ability to selectively implement functional blocks (*i.e.*, using parameter settings). Therefore, the skilled artisan would recognize that adding the Baldwin multiplexer to the pipeline stage of FIG. 1 would add to the area, cost and power of the processor of FIG. 1. These teachings, therefore, lead the skilled artisan away from the combination for the same reasons articulated by the Office Action as being important to the skilled artisan (*e.g.*, improved efficiency/flexibility, and reduction in unnecessary processing).

Respectfully, the skilled artisan would not look to add multiplexer circuitry to the pipeline stages of FIGs. 1 and 2 because the functionally alleged to be provided (*e.g.*, selective use of functional units) is already taught to be provided as either specifically designed pipelines or through parameter selection. Thus, the additional circuitry would unnecessarily complicate the circuit, leading the skilled artisan away from such a combination.

Notwithstanding, Applicant has made amendments to the claims in an effort to facilitate prosecution. For at least the reasons stated above these amendments are not believed to be necessary to overcome the rejections and Applicant reserves the right to claim similar subject matter in the future, such as through a continuation application. The claim amendments are generally directed toward the ability of routing auxiliary function

elements to multiple pipelines. To assist the Examiner, Applicant notes that support can be found in reference to Figures 3 and 5 and in the relevant discussion. These figures show a pool of auxiliary function blocks 330 which can be routed to multiple ones of pipelines 320a-320e. For example, a control register matrix 530 can be used to control the routing of the functional blocks. Auxiliary functional block A can be routed to multiple ones of the pipelines as determined by control register matrix 530.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-9068 (or the undersigned).

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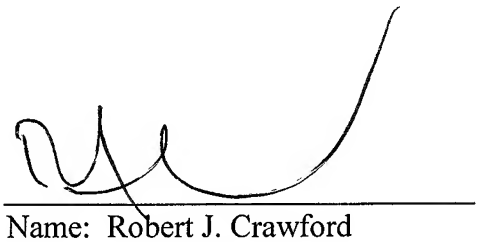
By: 

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